
DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the optical flip flop equipment to which flip-flop actuation is made to perform especially with an optical input signal about the semiconductor device which acquires an electric-generating-power signal to an optical input signal.
[0002]
[Description of the Prior Art] As a main element of a logic IC, although a counter, a shift register, memory, etc. can be mentioned, these are constituted by the flip-flop which memorizes 1-bit information. It is classified into a flip-flop according to the difference in a function with a set-reset mold (SR-FF), JK mold (JK-FF) which canceled the prohibition input in SR-FF, the toggle mold (T-FF) which outputs one half of the signals of a period of a clock signal, and the delayed type (D-FF) with which an input signal is delayed with a clock signal. Since especially the flip-flop of a set-reset mold can initialize the data which had the easiest structure, and latched data with the set signal, and were latched by the reset signal, it is used as a core of static memory.
[0003] The table of truth value is shown for the circuit diagram of SR-FF constituted from a conventional technique in drawing 10 in drawing 11 again. For S, in drawing 10 R> 0 and drawing 11 , a set signal and R are [an output and Q~ of a reset signal and Q] the reversal outputs of Q.
[0004] The flip-flop is used as various functional circuits in the conventional electronic circuitry. Therefore, in the optical computing and optical signal processing to which current research is progressing, the optical flip flop which operates with a lightwave signal is needed like the conventional electronic circuitry. Especially the optical flip flop of a set-reset mold attracts attention from the ability to use also as optical memory.
[0005]
[Problem(s) to be Solved by the Invention] The optical flip flop of SR mold which operates with a lightwave signal is realizable by adopting an optoelectric transducer called a photodiode as the input section of the flip-flop by the conventional electronic circuitry. However, conventionally, as shown in said drawing 10 , since there were many configuration element numbers, there was a problem that engine performance sufficient in the field of a degree of integration or a working speed was not obtained in a circuit.
[0006] The invention in this application is made in order to solve the problem of the conventional technique like the above, and it aims at raising a degree of integration and offering the optical flip flop equipment in which high-speed operation is possible.
[0007]
[Means for Solving the Problem] The invention in this application enables it to choose two stabilized points freely with a lightwave signal by making a bistability condition using two electronegative differential resistance elements (or it being the same a circuit and the following), and connecting an optoelectric transducer to juxtaposition at an electronegative differential resistance element. If such a configuration is used, since the same function is conventionally realizable with a very small element

number compared with the thing using a circuit, a degree of integration can be raised and the possible optical flip flop of high-speed operation can be realized.
[0008] first, the terminal which invention according to claim 1 connects an electronegative differential resistance element to 2 serials, and impresses driver voltage to the both ends -- moreover, it is the lightwave signal which prepared the output terminal at said both node, and was inputted into the optoelectric transducer by [of said electronegative differential resistance element] connecting an optoelectric transducer to juxtaposition at least at one of components, and said output terminal is made to realize a flip-flop function
[0009] Invention according to claim 2 the end of the terminal which impresses said driver voltage of invention of claim 1 Moreover, a predetermined high-voltage terminal, Use the other end as a predetermined low-battery terminal, and between said high-voltage terminals and output terminals, connect the 2nd optoelectric transducer, and the 1st optoelectric transducer is connected between said low-battery terminals and output terminals. An output terminal electrical potential difference is made to realize the flip-flop function of a set-reset mold by inputting an optical set signal into the 2nd optoelectric transducer, and inputting an optical reset signal into the 1st optoelectric transducer.
[0010] Invention according to claim 3 the terminal which impresses the driver voltage by the side of said 2nd electronegative differential resistance element Moreover, a predetermined high-voltage terminal, The terminal which impresses the driver voltage by the side of the 1st electronegative differential resistance element is used as a predetermined low-battery terminal. A load component is connected between said high-voltage terminal and the 2nd electronegative differential resistance element. The 2nd optoelectric transducer which inputs an optical set signal is connected to said 2nd electronegative differential resistance element at juxtaposition. Moreover, connect to juxtaposition the 1st optoelectric transducer which inputs an optical reset signal in the series circuit of said 1st and 2nd electronegative differential resistance elements, and input an optical set signal into the 2nd optoelectric transducer, and an optical reset signal is inputted into the 1st optoelectric transducer. It considers as the optical flip flop equipment of SR mold.
[0011] Moreover, the node of the 1st and 2nd optoelectric transducers of invention of said claim 3 is changed, like invention of claim 3, an optical set signal is inputted into the 2nd optoelectric transducer, it inputs an optical reset signal into the 1st optoelectric transducer, and invention according to claim 4 is taken as the optical flip flop equipment of SR mold.
[0012] Moreover, invention according to claim 5 uses two optical flip flop equipments according to claim 1. It has the series circuit which connected to 2 serials the parallel circuit which furthermore connected the source and the drain terminal of a field-effect transistor to the both ends of one electronegative differential resistance element. An output terminal is connected to the gate terminal of each field-effect transistor of said series circuit. each of said two optical flip flop equipments -- The node of said two parallel circuits is made into the output terminal of an electrical signal. For the driver voltage terminal of said two optical flip flop equipments It constitutes so that an oscillating electrical potential difference in phase may be impressed, a constant voltage may be impressed to the both ends of said series circuit and the same lightwave signal may be impressed to the optoelectric transducer which constitutes said 1st and 2nd optical flip flop equipment, and said output terminal is made to realize the flip-flop function of D mold.
[0013] Moreover, in claim 6, resonance tunnel diode (RTD) is used as an electronegative differential resistance element used for invention of claim 1 thru/or claim 5.
[0014]
[Function] Drawing 6 is the circuit diagram which carried out 2 series connection of the component or circuit which has an electronegative differential resistive characteristic for explaining the foundation of the invention in this application. In drawing 6 , an electronegative differential resistance element (for example, resonance tunnel diode) and OUT of RTD1 and RTD2 are output terminals. If the end of the circuit which carried out the series connection is grounded and the bias voltage (Vbias) of a direct current is impressed to the other end as shown in drawing 6 , the number of the stabilized points of an output state will change with the magnitude of this bias voltage.

[0015] Drawing 7 is the current-voltage characteristic Fig. of the circuit of drawing 6 . As shown in (a), when the peak voltage (****: electrical potential difference from which a current value serves as max) of the magnitude of direct-current bias voltage is smaller than twice (Vbias<2****), as for a stabilized point, only one of the S0 exists, but as shown in (c), a stabilized point is set to two, S1 and S2, in being larger than twice (Vbias>2****). These two stabilized points are made to correspond to a logical value "0" and "1."

[0016] In bias conditions (Vbias>2****) which will be in the bistability condition like the above As shown in drawing 8 , optoelectric transducers (for example, photodiode) PD1 and PD2 are connected to the electronegative differential resistance elements RTD1 and RTD2 at juxtaposition, respectively. By irradiating light and changing one of the current-voltage characteristics of a driving side to these optoelectric transducers PD1 and PD2 a load side, as shown in drawing 9 , the current-voltage characteristic can be modulated so that a stabilized point may be set to one.

[0017] In the example shown in drawing 9 , the increase of a component current (an alternate long and short dash line shows to drawing 9) and the trough current Iv of RTD1 are made larger than the peak current Ip (a continuous line shows a current characteristic to drawing 9) of the upper electronegative differential resistance element RTD2 by giving a lightwave signal to the optoelectric transducer PD 1 which connected with juxtaposition at the electronegative differential resistance element RTD1 of the drawing 8 bottom. For this reason, a stabilized point is set only to S1 and an output is set to "0." Since the potential barrier exists between S1 and S2 even if it removes the lightwave signal impressed to the optoelectric transducer PD 1 from this condition and returns to a bistability condition, an output is maintained with "0" (condition of S1).

[0018] Moreover, by giving a lightwave signal conversely to the optoelectric transducer PD 2 which connected with juxtaposition at the electronegative differential resistance element RTD2 of the drawing 8 top, a component current is increased and "1" can be chosen as an output by carrying out the ballet current of RTD2 beyond the peak current of the lower electronegative differential resistance element RTD1. Since the potential barrier exists between S1 and S2 even if it removes the lightwave signal similarly impressed to PD2 and returns to a bistability condition also in this case, an output is maintained with "1" (condition of S2). therefore, selection of "1" or "0" -- the upper and lower sides -- it is determined by to which optoelectric transducer a lightwave signal is impressed.

[0019] As mentioned above, an output is set to "1" (S2) whenever it impresses a lightwave signal to the optoelectric transducer PD 2 which the output was always set to "0" (S1), and connected with the upper electronegative differential resistance element RTD2 at juxtaposition when the lightwave signal was impressed to the optoelectric transducer PD 1 which connected with juxtaposition at the lower electronegative differential resistance element RTD1. Therefore, flip-flop actuation of SR mold is realizable with a lightwave signal.

[0020]

[Embodiment of the Invention]

(Gestalt of the 1st operation) Drawing 1 is the circuit diagram showing the gestalt of operation of the 1st of this invention, and shows the optical flip flop equipment of a set-reset mold. In drawing 1 , the component or circuit (it is hereafter described as the 1st electronegative differential resistance element) where 1 has the 1st electronegative differential resistive characteristic, and 2 are the components or circuits (it is hereafter described as the 2nd electronegative differential resistance element) which have the 2nd electronegative differential resistive characteristic, and show the example of resonance tunnel diode (RTD) here. 3 is the 1st optoelectric transducer, 4 is the 2nd optoelectric transducer, and the example of a photodiode (PD) is shown here. Moreover, as for an optical reset signal and 6, 5 is [an optical set signal and 9] output terminals. Moreover, 7 and 8 are driver voltage terminals, and the high voltage (Vdd) is impressed to 7 and they usually impress a low battery (Vss) to 8. Moreover, the peak current value of the electronegative differential resistance element 1 and the electronegative differential resistance element 2 supposes that it is the same.

[0021] Hereafter, actuation is explained. If the electrical potential difference corresponding to a logical value "1" will occur in an output terminal 9 if the optical set signal 6 is inputted into the 2nd optoelectric

transducer 4, and the optical reset signal 5 is inputted into the 1st optoelectric transducer 3 by the principle explained by said drawing 8 and drawing 9 R> 9, in an output terminal 9, the electrical potential difference corresponding to a logical value "0" will occur. Moreover, when there is no input of the optical set signal 6 and the optical reset signal 5, a logic state does not change. Moreover, when the optical set signal 6 and the optical reset signal 5 are inputted into coincidence, since an output is not decided, it considers as prohibition. The logic which was in agreement with the table of truth value shown in said drawing 1111 with the above-mentioned actuation can be acquired.

[0022] (Gestalt of the 2nd operation) Drawing 2 is the circuit diagram showing the gestalt of operation of the 2nd of the invention in this application, and drawing 3 is a voltage-current property Fig. for explaining the operating state. In drawing 2 , the same number was given to the part of the same function as drawing 1 . Different points from the gestalt of the 1st operation shown in drawing 1 R> 1 are the part which connects the 1st optoelectric transducer 3 into which an optical reset signal is made to input, and a point that a load 10 exists between the 2nd electronegative differential resistance element 2 and the drive terminal 7. In addition, although it is possible to use resistance, diode, FET, etc. as a load 10, the actuation at the time of using FET as a load component here is explained.

[0023] First, an electrical potential difference which the potential difference of 2 or more **** produces between a node 11 and the drive terminal 8 is impressed to the drive terminals 7 and 8. This condition is equivalent to B1 point of drawing 3 (namely, B one point potential of a node 11 correspondence). Therefore, the series circuit of the 1st electronegative differential resistance element 1 and the 2nd electronegative differential resistance element 2 will be in a bistability condition like the gestalt 1 of operation. If the optical set signal 6 is irradiated in this condition, a logical value "1" can be made to output to an output terminal 9 like the gestalt of the 1st operation.

[0024] Next, the case where a flip-flop is reset is explained. The load curve to the load 10 at the time of putting the 1st electronegative differential resistance element 1 and the 2nd electronegative differential resistance element 2 at one driver element is shown like drawing 3 . Therefore, if the optical reset signal 5 is irradiated by the 1st optoelectric transducer 3, the potential of a node 11 will change from B1 to a low battery like B-2 and B3. If it sets up so that B-2 and the potential of B3 may become smaller than 2**** here, the series circuit of the 1st electronegative differential resistance element 1 and the 2nd electronegative differential resistance element 2 will change from a bistability condition to S0 [in / in the potential of a monostable condition, i.e., an output terminal, / said drawing 7 (a) or (b)]. If the optical reset signal 5 goes out, since the potential of a node 11 is again set to B1, the potential of 2 or more **** will be supplied to the series circuit of the 1st electronegative differential resistance element 1 and the 2nd electronegative differential resistance element 2. Here, area of the 1st electronegative differential resistance element 1 is made a little larger than the area of the 2nd electronegative differential resistance element 2, and if the peak current value of the 1st electronegative differential resistance element 1 is set up so that it may become larger than the peak current value of the 2nd electronegative differential resistance element 2, in case it will transfer to a bistability condition from a monostable condition, an output terminal 9 can surely be made into the potential corresponding to a logical value "0."

[0025] (Gestalt of the 3rd operation) Drawing 4 is the circuit diagram showing the gestalt of operation of the 3rd of this invention. A different point from the gestalt of said 2nd operation is that the connection places of the optoelectric transducer which inputs the optical set signal 6 and the optical reset signal 5 differ. Since fundamental actuation is similar with the gestalt of the 2nd operation, it is explained below about a different point.

[0026] With the gestalt of this operation, when the optical set signal 6 is inputted, the potential of a node 11 decreases. The electrical potential difference impressed to the series circuit of the 1st electronegative differential resistance element 1 and the 2nd electronegative differential resistance element 2 by this is set to 2 or less ****, and an electronegative differential resistance element series circuit is transferred from a bistability condition to a monostable condition. Then, if the optical set signal 6 is turned off, it will return from a monostable condition to a bistability condition again, but in that case, the peak current value of the 2nd electronegative differential resistance element 2 is set up so that it may become larger

than the peak current value of the 1st electronegative differential resistance element 1, so that a logical value "1" may always be outputted. What is necessary is just to distinguish between the area of an electronegative differential resistance element like the gestalt of the 2nd operation, in order to give change to the peak current value of two electronegative differential resistance elements. In addition, the actuation at the time of reset is the same as that of the gestalt of said 2nd operation.
[0027] (Gestalt of the 4th operation) Drawing 5 is drawing showing the gestalt of operation of the 4th of the invention in this application, (a) is a circuit diagram and (b) is the timing diagram of a signal. here -- 21 thru/or 24 -- a high-voltage terminal and 34 show a low-battery terminal, and, as for the 1st and 2nd optoelectric transducers, and 27 and 28, in the 1st thru/or the 4th electronegative differential resistance element, and 25 and 26, 35 shows an output terminal, as for the 5th and the 6th electronegative differential resistance element, a lightwave signal with the 1st and 2nd field-effect transistors (FET), and 31 and 32, and 33. [same / 29 and 30]
[0028] Moreover, the circuit element of A and B enclosed with a broken line connects an optoelectric transducer to one of electronegative differential resistance elements, and juxtaposition in the series circuit of two electronegative differential resistance elements. Two electronegative differential resistance elements by which series connection was carried out here have given change to the mutual peak current value. for example, if a circuit element A is explained as an example, when a lightwave signal will not be inputted into an optoelectric transducer 26 The peak current value of the electronegative differential resistance element 23 to which the optoelectric transducer is not connected is larger than the current value near the peak voltage of the current which flows the juxtaposition section of an optoelectric transducer 26 and the electronegative differential resistance element 24. Moreover, when a lightwave signal is inputted into an optoelectric transducer 26, it is set up so that the current value near the peak voltage of the current which flows the juxtaposition section of an optoelectric transducer 26 and the electronegative differential resistance element 24 may become larger than the peak current value of the electronegative differential resistance element 23 to which the optoelectric transducer is not connected. The same is said of a circuit element B. Furthermore, the oscillating electrical potential difference of the same phase is impressed to the Vbias terminal of circuit elements A and B, and what has the bigger peak value of an oscillating electrical potential difference (Vbias) than 2**** is used. Although it transfers from a monostable condition to a bistability condition in case the magnitude of this oscillating electrical potential difference serves as Vbias>2****, a logical value "0" or "1" can be chosen by the difference in the peak current value in the load component and driver element in the transition point.
[0029] The circuit element of the part C enclosed with a broken line is the series circuit which connected to 2 serials the parallel circuit which connected the source and the drain terminal of a field-effect transistor to the both ends of one electronegative differential resistance element, a constant voltage is impressed to both ends and the output terminal of said circuit elements A and B is connected to the gate terminal of said two field-effect transistors, respectively. If a signal is impressed to the gate of one of field-effect transistors, the current-voltage characteristic of a field-effect transistor and an electronegative differential resistance element is set up here so that it may change from a bistability condition to a monostable condition like drawing 4 .
[0030] An output terminal 25 can be made to realize the flip-flop function of D mold in such a circuit by inputting the same lightwave signal into two optoelectric transducers 25 and 26 at coincidence. Since a circuit element A will output "1" and a circuit element B will specifically output "0" if the oscillating electrical potential difference (Vbias) which drives circuit elements A and B becomes larger than 2**** when there is a lightwave signal input, a field-effect transistor 30 serves as ON, and "1" appears in an output terminal. Even if the oscillating electrical potential difference (Vbias) which drives circuit elements A and B in this condition decreases, since the output of a circuit element C is latched, it does not change. Since a circuit element A outputs "0" and a circuit element B outputs "1" when a lightwave signal is not inputted at the point which an oscillating electrical potential difference increases similarly, a field-effect transistor 29 serves as ON, and "0" appears in an output terminal. It turns out that it comes to be shown in drawing 5 (b) when the above actuation is indicated to a timing diagram, and the gestalt

of this operation carries out flip-flop actuation of D mold.
[0031] In addition, in the gestalt of the operation explained until now, although the case where used resonance tunnel diode as an electronegative differential resistance element or a circuit, and a photo transistor was used as an optoelectric transducer was illustrated, even if it uses other equivalent components and circuits, the invention in this application can be constituted similarly.
[0032]
[Effect of the Invention] As mentioned above, since the circuit which carries out flip-flop actuation with an optical input signal can be constituted from some electronegative differential resistance elements according to the invention in this application as explained, the circuit which has the same function with a very small element number compared with a component conventionally is realizable. Furthermore, since the capacity component is very small and its high-speed operation is possible for the resonance tunnel diode which was used here in addition to a configuration element number being made few, the effectiveness that high-speed optical flip flop equipment is extremely realizable is acquired.

[Translation done.]

DERWENT-ACC-NO: 1999-239738

DERWENT-WEEK: 199920

TITLE: Optical flip=flop circuit for e.g. semiconductor device - has photodiode for inputting light signal, and which is connected in parallel to each resonant tunneling diode, such that resonant tunneling diodes are connected in series

PATENT-ASSIGNEE: NIPPON TELEGRAPH & TELEPHONE CORP[NITE]

PRIORITY-DATA: 1997JP-0214584 (August 8, 1997)

PATENT-FAMILY:

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JP 11068521 A	March 9, 1999	N/A	008	H03K 003/315

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 11068521A	N/A	1997JP-0214584	August 8, 1997

INT-CL (IPC): H03K003/315

ABSTRACTED-PUB-NO: JP 11068521A

BASIC-ABSTRACT:

NOVELTY - A photodiode (3,4) for inputting a light signal, is connected in parallel to each resonant tunneling diode (1,2). The resonant tunneling diodes are connected in series. DETAILED DESCRIPTION - A drive voltage terminal (7,8) is provided at one end of each resonant tunneling diode. A drive voltage is applied to each resonant tunneling diode through the drive voltage terminals. An output terminal (9) that is connected to the common node of the resonant tunneling diodes, enables the output of an electrical signal.

USE - For e.g. semiconductor device.

ADVANTAGE - Obtains an optical flip-flop circuit having lesser number of components. Improves the operating speed of the optical flip-flop circuit. DESCRIPTION OF DRAWING(S) - The figure shows the circuit diagram of the optical flip-flop circuit. (1,2) Resonant tunneling diode; (3,4) Photodiode; (7,8) Drive voltage terminal; (9) Output terminal.

CHOSEN-DRAWING: Dwg.1/11

TITLE-TERMS: OPTICAL FLIP=FLOP CIRCUIT SEMICONDUCTOR DEVICE PHOTODIODE INPUT LIGHT SIGNAL CONNECT PARALLEL RESONANCE DIODE RESONANCE DIODE CONNECT SERIES

DERWENT-CLASS: U22

EPI-CODES: U22-A02C; U22-A04C;

SECONDARY-ACC-NO:

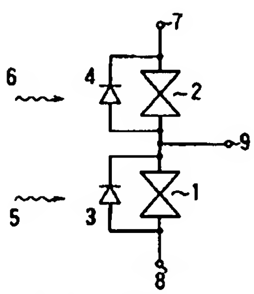
Non-CPI Secondary Accession Numbers: N1999-179004

3…第1の光電変換素子（PD）
4…第2の光電変換素子（PD）
5…光リセット信号
6…光セット信号
7、8…駆動電圧端子
9…出力端子
10…負荷
11…接続点
21…第1の負性微分抵抗素子（RTD）
22…第2の負性微分抵抗素子（RTD）
23…第3の負性微分抵抗素子（RTD）

24…第4の負性微分抵抗素子（RTD）
25…第1の光電変換素子（PD）
26…第2の光電変換素子（PD）
27…第5の負性微分抵抗素子（RTD）
28…第6の負性微分抵抗素子（RTD）
29…第1の電界効果トランジスタ（FET）
30…第2の電界効果トランジスタ（FET）
31、32…光信号
33…高電圧端子
34…低電圧端子
35…出力端子

【図1】

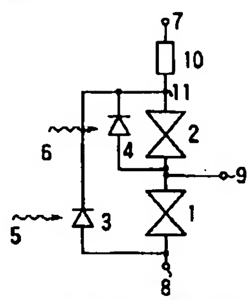
(図1)



1…第1の負性微分抵抗素子
2…第2の負性微分抵抗素子
3…第1の光電変換素子
4…第2の光電変換素子
5…光リセット信号
6…光セット信号
7、8…駆動電圧端子
9…出力端子

【図2】

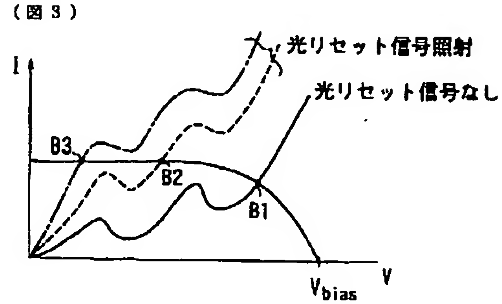
(図2)



1…第1の負性微分抵抗素子
2…第2の負性微分抵抗素子
3…第1の光電変換素子
4…第2の光電変換素子
5…光リセット信号
6…光セット信号
7、8…駆動電圧端子
9…出力端子
10…負荷
11…接続点

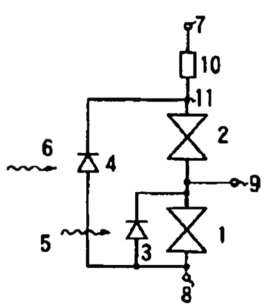
【図3】

(図3)



【図4】

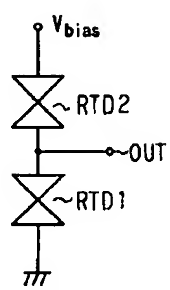
(図4)



1…第1の負性微分抵抗素子
2…第2の負性微分抵抗素子
3…第1の光電変換素子
4…第2の光電変換素子
5…光リセット信号
6…光セット信号
7、8…駆動電圧端子
9…出力端子
10…負荷
11…接続点

【図6】

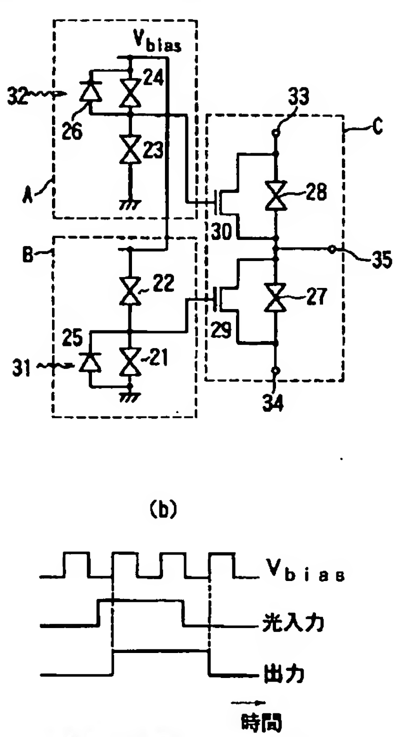
(図6)



RTD1、RTD2…負性微分抵抗素子
（共鳴トンネルダイオード）
OUT…出力端子

【図5】

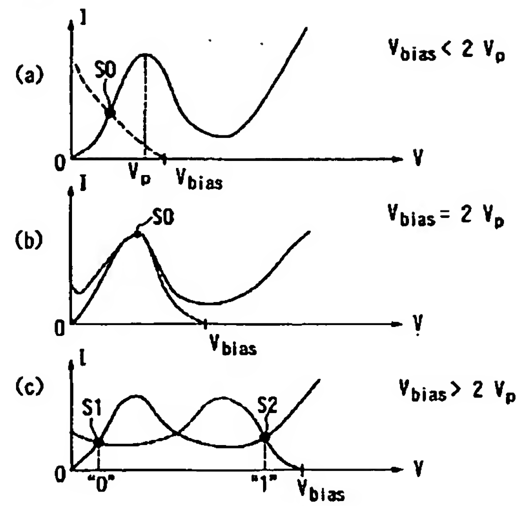
（図５）



２１～２４…負性微分抵抗素子
２５、２６…光電変換素子　２７、２８…負性微分抵抗素子
２９、３０…電界効果トランジスタ　３１、３２…光信号
３３…高電圧端子　３４…低電圧端子　３５…出力端子

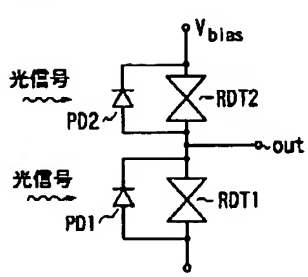
【図7】

（図７）



【図8】

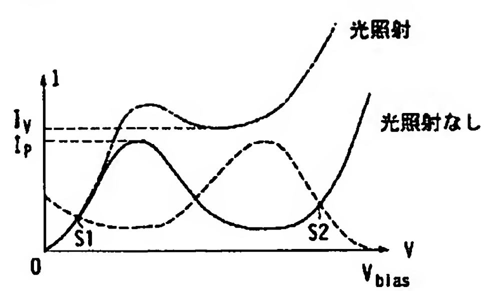
（図８）



ＲＴＤ１、ＲＴＤ２…負性微分抵抗素子
（共鳴トンネルダイオード）
ＰＤ１、ＰＤ２…光電変換素子
（フォトダイオード）
ＯＵＴ…出力端子

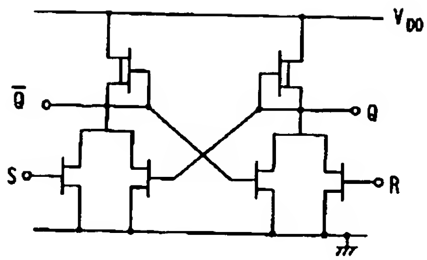
【図9】

（図９）



【図10】

(図10)



【図11】

(図11)

S	R	Q	$\overline{Q}$	
0	0	変化せず		
1	0	1	0	… "SET"
0	1	0	1	… "RESET"
1	1	禁止		

OPTICAL FLIP-FLOP DEVICE

Patent number:	JP11068521
Publication date:	1999-03-09
Inventor:	AKEYOSHI TOMOYUKI
Applicant:	NIPPON TELEGRAPH & TELEPHONE
Classification:	
- international:	H03K3/315
- european:	
Application number:	JP19970214584 19970808
Priority number(s):	JP19970214584 19970808

Abstract of **JP11068521**

PROBLEM TO BE SOLVED: To provide an optical flip-flop device that improves the degree of integration and enables operation at a high speed. SOLUTION: Negative differential resistor elements 1 and 2 are serially connected, and terminals 7 and 8 which apply a drive voltage to the both ends are provided. An output terminal 9 is provided with connection points of both elements 1 and 2. Also by connecting photoelectric transducers 3 and 4 to at least one element of the negative differential resistor elements 1 and 2, a flip-flop function is provided with an output terminal 9. For example, an optical signal 5 is made to be an optical resetting signal, and an optical signal 6 is made to be an optical setting signal.